FULL ADDER

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To reduce delay in Critical Path and Simultanious Reduction in Power Dissipation is ultimate AIM of Choice of ADDER CIRCUIT ONE SHOULD USE.

Using XOR & AND GATES ONE needs 32 Transistors to Implement 1 Bit Adder which also takes Carry Input.

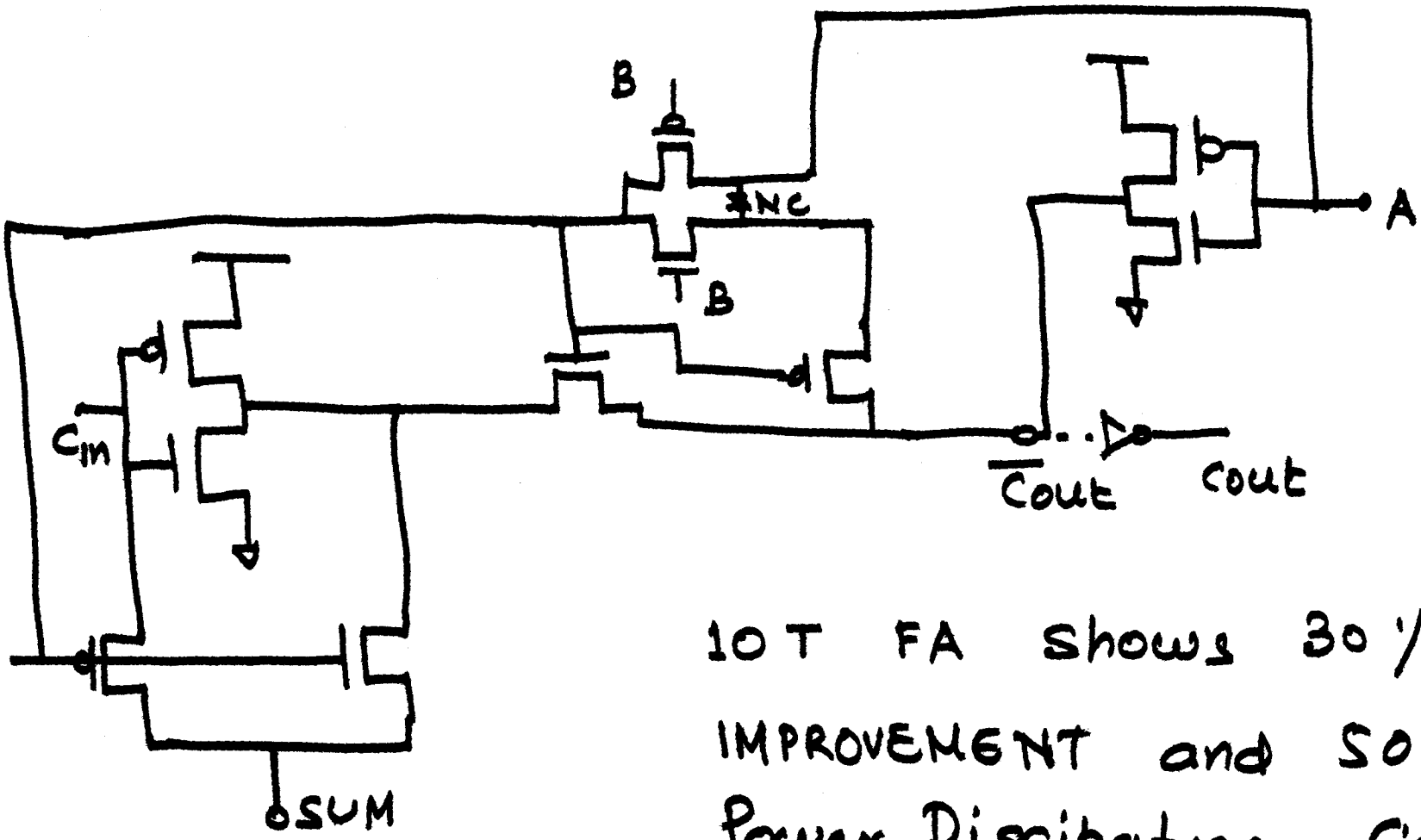
IN QUEST OF BETTER SPEED A LOWER POWER DISSIPATION, MANY FULL ADDER CIRCUIT IMPLEMENTATIONS HAVE BEEN TRIED like 17 Transistor FA, 14 Transistor FA and 10 Transistor FA.

A 10-T FA is as shown in next Slide

If We expand XOR Function & then Represent SUM & $Carry_{OUT}$ in terms of ONLY AND/OR GATES, we CAN REDUCE TRANSISTOR COUNT AS WELL AS DELAY IN CRITICAL PATH

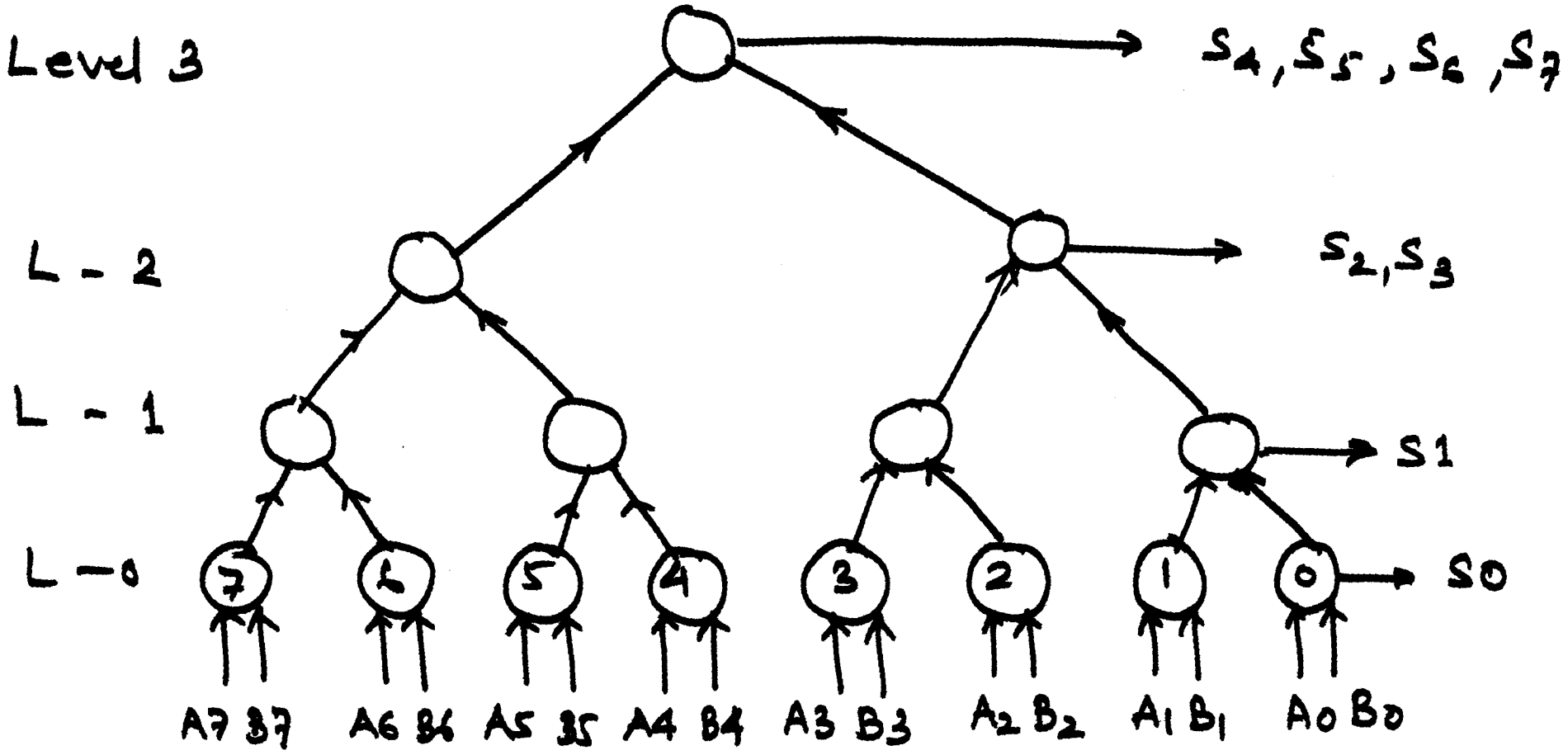
A 28 Transistor Full Adder is one such Adder.

A 10-Transistor FULL ADDER



10T FA shows 30%. SPEED IMPROVEMENT and 50%. lower Power Dissipation COMPARED ANY OTHER TFA.

ELM ALGORITHM USING BINARY TREE
8-Bit Adder (CLA)



Comparision Between Various Adders of 32 Bits

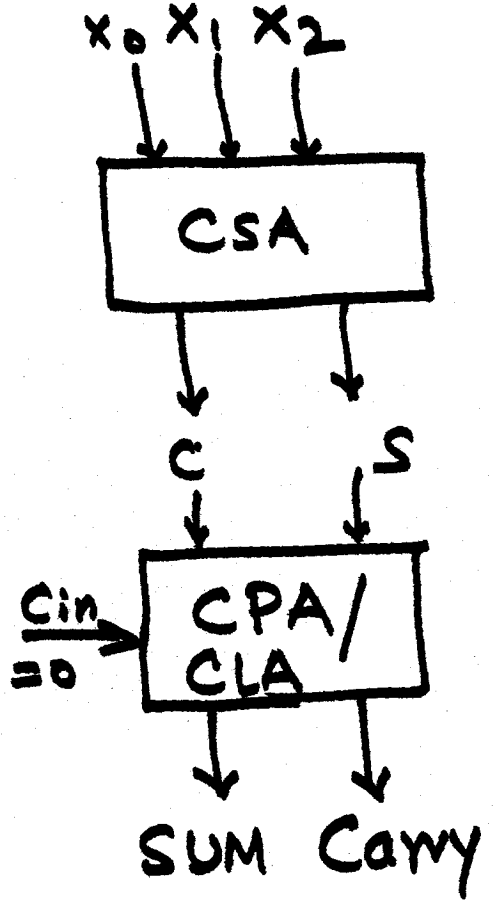
SPECS:
$V_{DD} = 3.3\,V$, Clock Frequency = 100 MHz

Type	Area ($10^6 \lambda^2$)	No. of Transistors	Delay ns.	Av. P. Dissipation (mW)
CLA	2.27	2132	15	114.6
ELM	2.36	2078	10	104.1
RCA	0.80	1204	55	87.2

Cleorly ELM Binary Tree Adder is
BETTER ON PERFORMANCE & Power Dissipation

CARRY SAVE ADDER

Example :



Decimal Nos. as example : x y z are Three Numbers

Add

	1	1	1		
x	4	3	2	0	1
y	0	1	6	7	2
x_2	2	8	6	4	3
SUM :-	7	3	5	1	6

Cout = 0

Two Steps :

(i) Evaluate $S = X + Y + 2$ without taking Carry generated

X		4	3	2	0	1
Y		0	1	6	7	2
Z		2	8	6	4	3
S =	6	2	4	1	6	

(ii) Evaluate C by finding Carry generated for each column and placing it as next column input

X	4	3	2	0	1
Y	0	1	6	7	2
Z	2	8	6	4	3
C =	0	1	1	1	0

Binary No Example : Three Nos. X, Y, Z

	1 1 1 1	
X =	1 0 1 1 0 1	45
Y =	1 1 0 0 0 1	49
Z =	0 1 1 1 0 0	28
SUM	1 1 1 1 0 1 0	122
Cout →		

(1) Step I : Evaluate S (without use of Carry)

X	1 0 1 1 0 1
Y	1 1 0 0 0 1
Z	0 1 1 1 0 0
S =	0 0 0 0 0 0

(ii) Add S and C (shifted by left Position) to get SUM & Cout

S		6	2	4	1	6
C	0	1	1	1	0	
SUM	0	7	3	5	1	6

Cout = 0

This number is Same as what Normal Addition Gets.

(ii) step II : Evaluate C

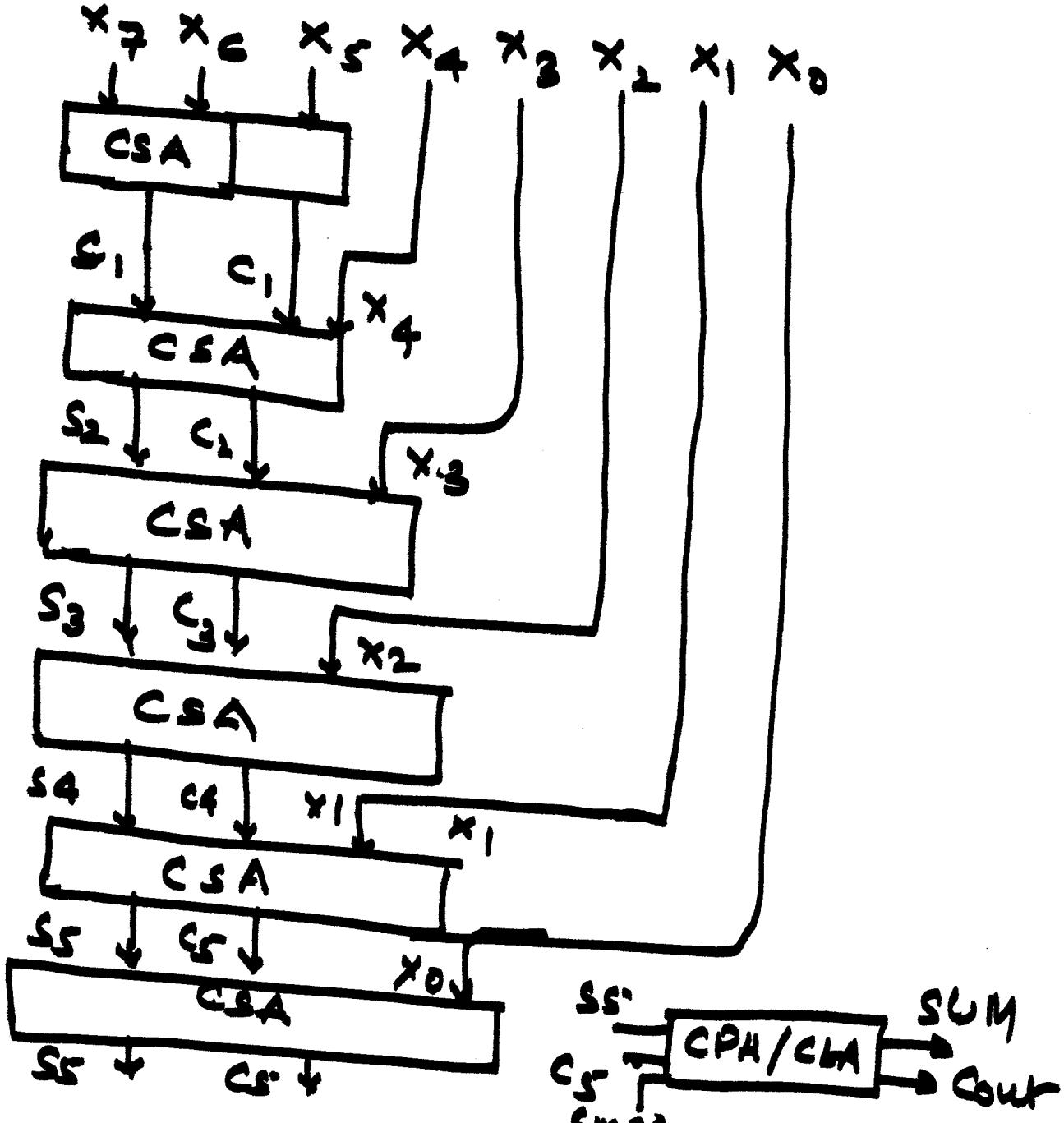
X		1	0	1	1	0 1
Y		1	1	0	0	0 1
Z	0	1	1	1	0	0
C	1	1	1	1	0	1

(iii) Add S and Left shifted C as above

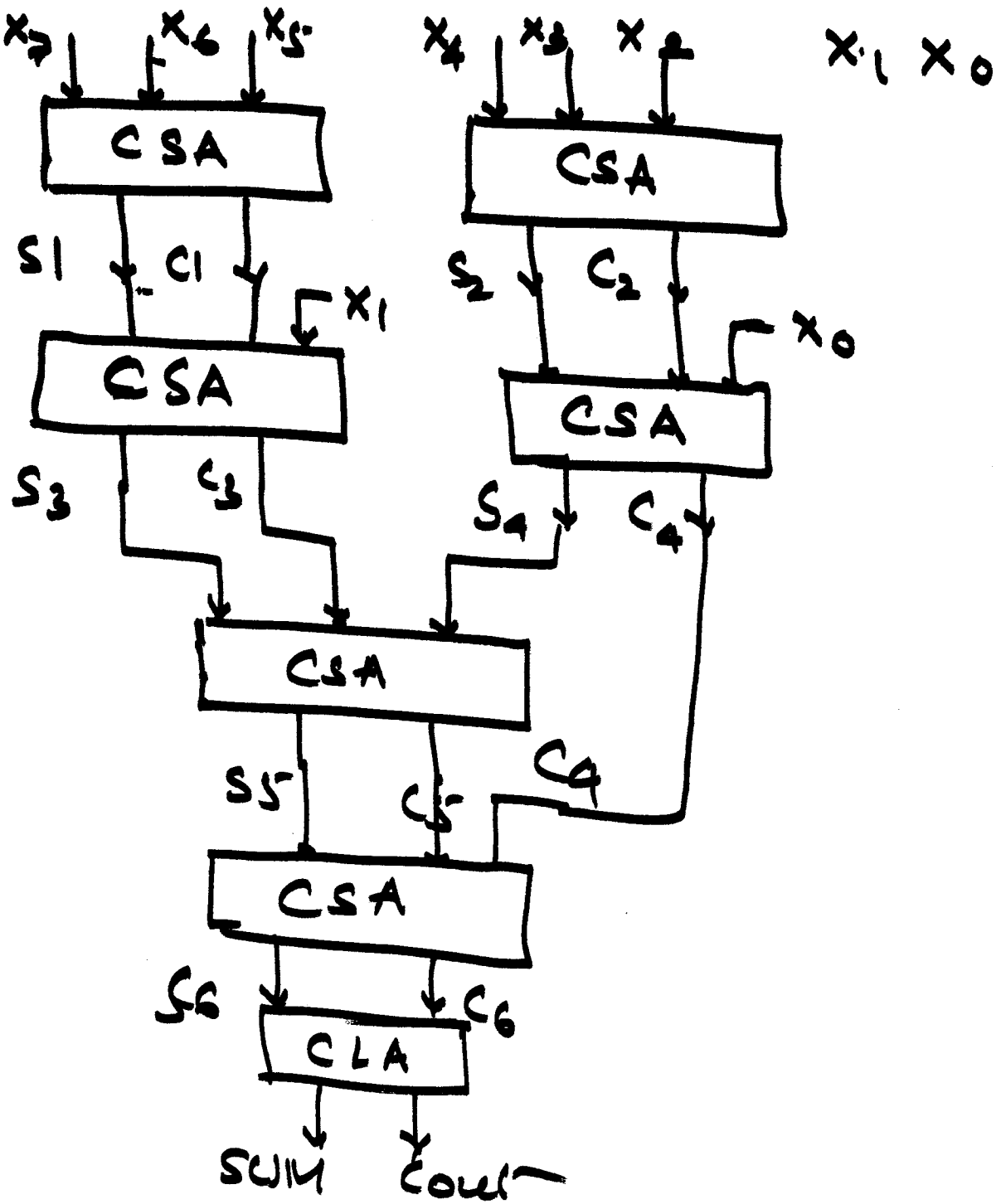
S	0	0	0	0	0	0	
C	1	1	1	1	0	1	
SUM	1	1	1	1	0	1	0 → 122 in Decimal

Cout

TREE ADDER : 8 bit CSA



WALLACE TREE



CURRENT MODE ADDERS

Instead of Voltage Mode Operation for Digital & Mixed-Signal Circuits, we can also use Current Mode Design methodology.

Current Mode Logic was a great candidate for Low Power High Speed VLSI Circuits.

Most DSP chips uses Recursive Technique based Algorithms. In these Systems it is observed that 70% of Chip Area is dedicated to Interconnects and 30% to Logic Devices. It is also advisable to use Multi Valued Logic based data to transmit on Single Wire. In Voltage Mode this is very Difficult. Hence Current Mode Signaling is used.

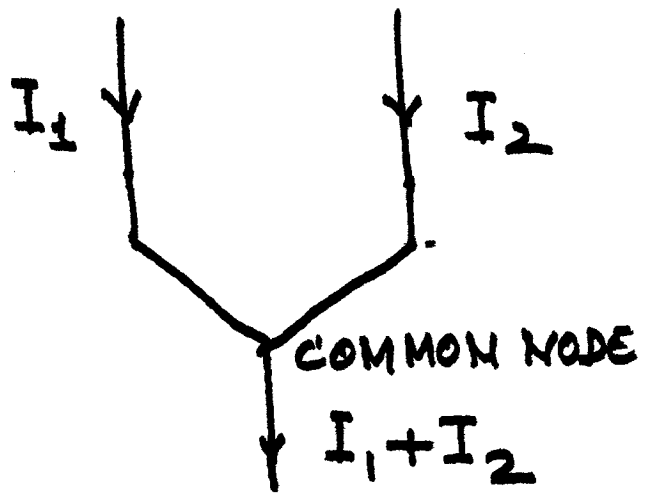
A 4 Digit DECIMAL ADDER

1. USES CURRENT MODE (MULTI-VALUED LOGIC)

2. It has 4 SDDA Cells
   (Single Digit Decimal Adder)

3. EACH SDDA CELL CONTAINS
   ONE CURRENT COMPARTOR (CC)
   & FIVE CURRENT MIRRORS

PRINCIPLE :—



If I_1 represents First input Decimal No. A & I_2, the Second Decimal no. B

Then Wiring as above will produce Addition of A and B at the COMMON NODE.

TYPICAL SDDA CELL

1. Two Current Mirrors USES 'SUPER MOS TRANSISTORS'. ST_n & ST_p are TWO SUCH MIRRORS.

2(b) SUPER MOS IS A 22 Transistor Circuit which uses Folded CASCODE STRUCTURE TO IMPROVE OUTPUT RESISTANCE to values which can recreate Ideal Current Sources ($R_{out} \rightarrow \infty$)

2. It uses TWO CURRENT MIRRORS WHICH ARE HIGH SWING CASCADED CURRENT MIRRORS. HS_n & HS_p are such MIRRORS with n & p type of Transistors Mirrors

3. Typical Decimal Digit is represented by Current Levels.

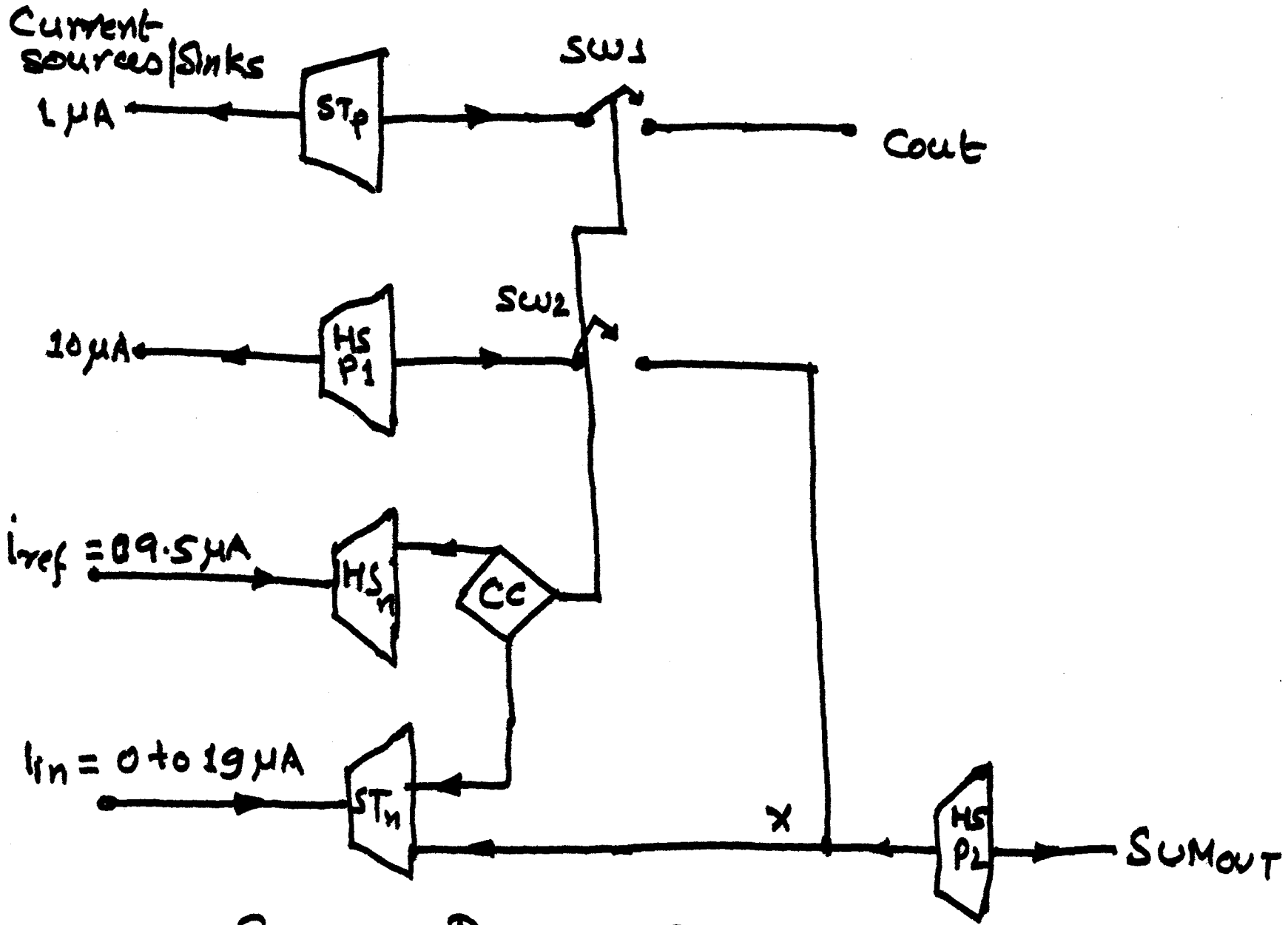
0 μA, 1 μA, 2 μA ---- 9 μA will represent nos. 0, 1, 2 ---- 9 in Decimal.

4. For 4-digit Adder I_{in} varies from 0 to 19 μA & Cout is Either 0μA or 1 μA (Decimal 0 or 1)

SDDA Implements PARTIAL SUM & Cout-

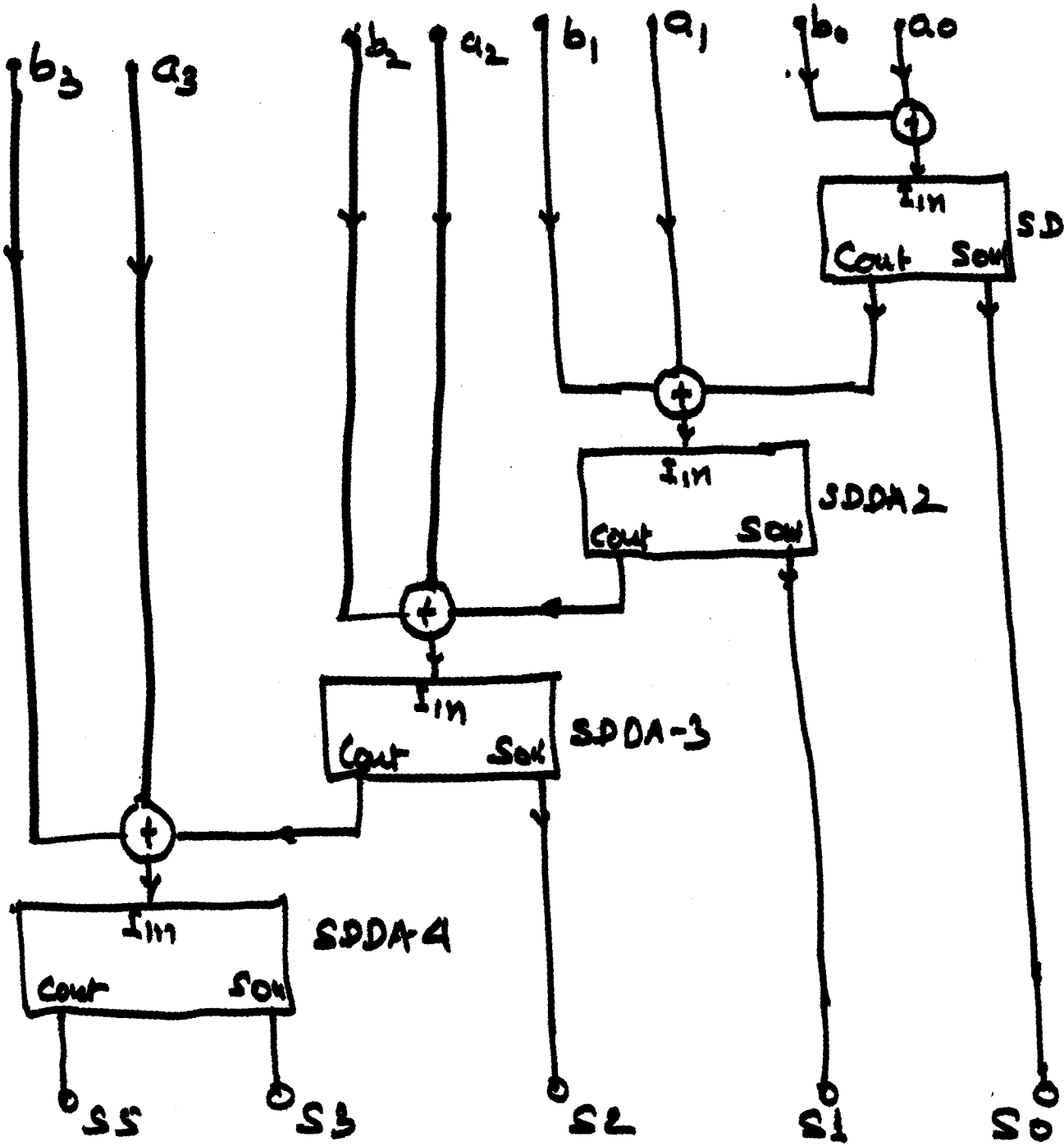
$$S_{out} = \begin{cases} I_{in} & \text{if } I_{in} \leq 9 \\ I_{in} - 10 & \text{if } I_{in} \geq 10 \end{cases}$$

$$C_{out} = \begin{cases} 0 & \text{if } I_{in} \leq 9 \\ 1 & \text{if } I_{in} \geq 10 \end{cases}$$



SINGLE DIGIT DECIMAL ADDER

Radnovik et al
IEEE conf. EIACE, 1996



4 DIGIT DECIMAL ADDER

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